STATEK

TECHNICAL NOTE

CIRCUIT BOARD LAYOUT CONSIDERATIONS FOR PIERCE OSCILLATORS

For proper operation and optimum performance of a Pierce oscillator, the circuit board layout should be designed to reduce:

a) The capacitances across the crystal (C_S) and the inverter (C_F).
b) The coupling of switching signals into the oscillator circuitry.
c) The capacitance from the input of the inverter to ground (C_I).

Considerations

Reducing the capacitance across the crystal and the inverter increases loop gain, reduces start time, and improves short-term stability.

Decreasing the input capacitance to ground increases the tuning range of the oscillator, reduces crystal drive level, and increases loop gain.

Isolating switching signals from the oscillator improves short-term stability.

Reducing coupling of switching signals to the oscillator decreases the possibility of spurious oscillation.

Layout Objectives

Eliminate parallel traces.
Keep trace lengths short.
Use ground traces to isolate signals.
Keep components separated to reduce coupling between component bodies.

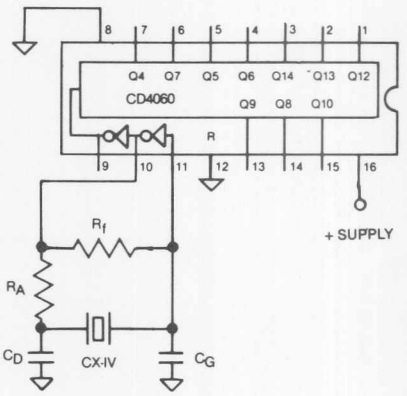

Figure 1 - Oscillator/Divider

Example:

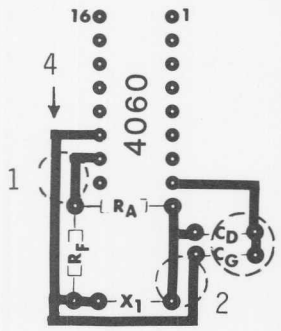

Figure 2 - Poor Layout

1. Parallel traces increase input to output capacitance (C_F).
2. Parallel traces increase capacitance across crystal (C_S).
3. Capacitance between bodies of C_D and C_G increase capacitance across crystal (C_S).
4. Excessively long traces on the input of the inverter increase the input capacitance.

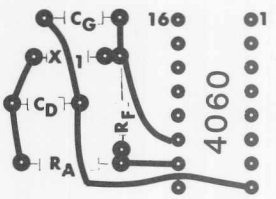

Figure 3 - Improved Layout

1. Traces are short and not parallel.
2. A ground trace is used to reduce the capacitance across the crystal (C_S). and to isolate the buffer output (Pin 9) from the oscillator circuitry.

12/87